Transmitter and Receiver

Patent No. 6,512,759 (U.S.), Patent No. 3096020 (Japan)

The present invention relates to an interleaving technique for digital modulation and demodulation, especially to a transmitter and a receiver capable of performing unified interleave and deinterleave corresponding to a multiplexing scheme based on any combination of transmission modes with different error endurances.

Japan started a digital satellite broadcasting service over seven HDTV channels in 2000. Fourty-eight distinct slots are employed in the digital multiplexed transmission signal, in which a maximum of four types of transmission mode can be simultaneously assigned to each slot to get a sufficient transmission capacity for HDTV and to overcome shut-off problems due to heavy rain attenuation.

The transmission signal must be subjected to interleaving in the transmitter and deinterleaving in the receiver in order for Reed-Solomon (RS) codes, by dispersing long burst errors, to have the maximum effect. In the conventional technique, the capacity of the FIFO (First In First Out) memory used for interleaving or deinterleaving depends on the assigned slot number for each of the transmission modes in the frame, and a complicated controller for the interleave process should be used because the address control is altered when the FIFO memory capacity that deals with a specific transmission mode changes, thereby complicating the circuitry.

The present invention was made to overcome the above-mentioned circuit complexity problems and employs a super frame structure to perform the interleave or deinterleave.

The transmission system permits different types of transmission mode with a frame structure consisting of N packets. The interleave frame is formed by combining slots corresponding to the same slot number in each frame during one super frame. The interleaving is performed every super frame by using only one memory control, even though mixed data with various transmission modes may be transmitted.

Figure 1 shows the structure of the super frame of this invention. The super frame has eight frames, and each frame consists of 48 slots. Various signal types, such as multiplexed signals including video, audio, and associated information are assigned to these slots as an MPEG-TS packet. Up to four kinds of transmission mode in one frame can be assigned to each slot. One slot consists of 204 (= 188+16) bytes so as to fit the MPEG-TS packet and RS parity.

The interleaving of the data in the super frame is performed using a memory that has a capacity of 203X8 bytes. The data, except for each packet synchronizer, is written into the memory in the horizontal direction, and the data is read out from the memory in the time-axis direction, as is shown in the figure. Furthermore, by exchanging the readout direction and the write direction, deinterleaving can be performed in the receiver.

Thus, the invention makes it possible to obviate memory address controllers complicated by the transmission mode structures of the interleave or the deinterleave process, thereby enabling a uniform control in any case.