

Development of a 1080/300p HDTV High Speed Camera Using Three 2.2 M-pix CMOS Image Devices

T. OGASAWARA¹, J. YAMAZAKI¹, Y. TOMURA¹, H. TANAKA¹, M. YAMAUCHI¹

Y. HASHIMOTO², H. CHO³, S. KANAYAMA⁴

JAPAN BROADCASTING CORPORATION (NHK), Tokyo, JAPAN¹

nac IMAGE TECHNOLOGY Inc., Tokyo, JAPAN²

Matsushita Electric Industrial Co., Ltd., Tokyo, JAPAN³

FUJINON Co., Ltd., Tokyo, JAPAN⁴

Abstract

We have developed an HDTV high speed camera that uses three 2.2 M-pixel CMOS (Complementary Metal Oxide Semiconductor) image devices. The camera enables image acquisition up to a maximum speed of 300 fps (frames/second) and stores the image sequences directly in a semiconductor memory in the camera head. Slow motion playback is available with a high picture quality as the image sequence is stored without compression. The compact, lightweight, handheld camera can be controlled from a CCU (Camera Control Unit) with a single standard HDTV hybrid camera cable.

Introduction

NHK developed the first HDTV high speed camera in 1992.¹⁾ This camera adopted three HARP (High-gain Avalanche Rushing Amorphous Photoconductor) tubes for image sensing and could capture the image at a rate of 180 fields/second. It provided high sensitivity by amplifying the signal within the tubes. This was used in athletics coverage of the 100 m race at the Barcelona Olympic Games. The problem was that the semiconductor memory block for storing a 30-second picture at 3 times normal speed weighed more than 200 kg, and the whole system about 216 kg.

In 1998, the second HDTV high speed camera was developed with the use of 130 M-pixel CCDs.²⁾ Of four CCD sensors, two were used for G channel, each driven at 1.5 times the speed of a normal HDTV camera. The outputs of two G-channel CCDs were read out alternately for each field (i.e. half frame), and thus achieved image pickup at 180 fields/second. This high speed camera was used for the ski jump coverage at the Nagano Winter Olympic Games and drew attention for its high-quality pictures. It required a large operating system with three CCUs and three VCRs mounted in two racks, however, weighed 200 kg in total and had a power consumption of 3 kW.

In this development project, we aimed to make a camera system that would be easy to operate and have a size and weight similar to those of normal HDTV camera systems, picture resolution of the 2.2 M-pixel

level, and maximum image pickup speed of 5 times normal speed.

The high-resolution 5x high speed camera is very effective in various situations. In sports programs, it can provide instant slow motion playback. In drama, it can make scale models look real by shooting them at high speed and playing back the images in slow motion. Use of a 5x high speed camera in special effects can, for example, make a 1/25 scale model look entirely real.

In this paper, we introduce the system configuration and features of our development and also some examples of how it has been used already in program production.



Photo 1: Appearance of the High Speed Camera

Development Concept

The image sensing block and memory block are the two major elements that determine the performance of high speed cameras in the readout and storage of images at high speed.

The three chip color method was adopted for the image sensing block, thereby enabling us to reduce light loss, in preference to the single chip color method. With respect to picture quality, too, this ensures sufficient color reproduction when the camera is used together with other broadcast cameras in multi-camera operation.

The CMOS sensor was adopted for image sensing for its low power consumption and suitability for high-speed readout. This sensor is capable of processing a vast amount of data without degradation by means of

parallel signal readout via multiple lines. Compared to the CCD (Charge Coupled Device), the CMOS sensor has problems of noise. Digital noise reduction circuitry was employed in the system to overcome this.

With regard to storage media, use of a semiconductor memory is suitable for high speed cameras because of the rapidity of data access. A versatile DIMM (Dual Inline Memory Module) SDRAM (Synchronous Dynamic Access Memory) was adopted for the camera memory on these grounds. Recent advances in semiconductor memory have enhanced the integration and enabled us to install a 20 GB-class memory in the camera head. This is the memory capacity needed to play back HDTV signals at a speed of 60 frames/second for about one minute.

The images are stored progressively without compression (RGB=4:4:4). In order to retain the vertical resolution of slow-motion and stop-motion pictures, the playback image data is processed progressively as well. Both 1080/60p (progressive scanning) and 1080/60i (interlace scanning) signals are output simultaneously from the CCU; the former is suitable for post-production activity such as CG composite work, and the latter for the broadcast itself.

System Configuration

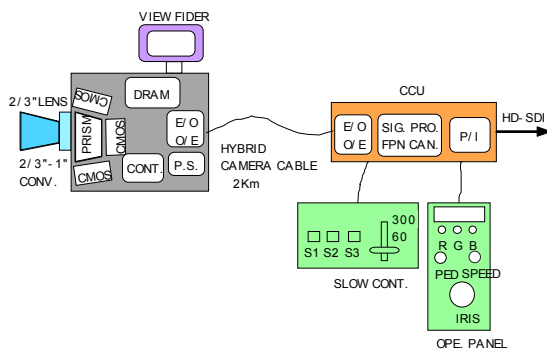


Figure 1: System Configuration

The high speed camera system introduced in this paper consists of two major parts, as shown in Figure 1; the camera head equipped with image device and memory, and CCU (camera control unit), which performs the final signal processing. The camera head and CCU can be connected with a single standard HDTV hybrid camera cable. The return video (RET) and power supply to drive the camera head are sent from the CCU to the camera head. The HDTV 1080/60p video and audio signals are sent from the camera head to the CCU. Other communication signals, such as intercom and tally, are transmitted in both directions.

Two controllers can be connected to the CCU for remote control, one to adjust the camera and the other to control the playback speed.

Image Sensing Block (CMOS)

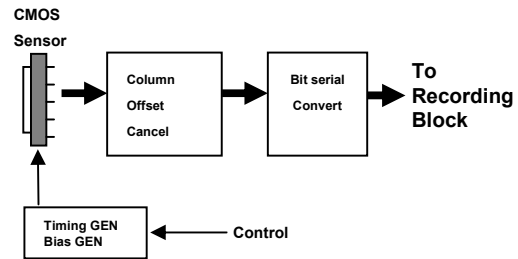


Figure 2: Block Diagram for Image Sensing

The CMOS sensor has the on-chip integrated functions of light-receiving sensor, analog signal processing circuit, A/D converting circuit etc.. Two analog signals are output from each pixel for the elimination of noise; an image signal which includes noise, and the noise itself which is the data acquired when there is no image. These signals are preserved in the column-parallel sample-and-hold (S&H) circuit. The S&H circuit outputs are subtracted and A/D converted to be written into a SRAM in columns. Each column's data undergoes offset compensation and is written into another SRAM. The signal is read out in parallel at a rate of 10 bits from 16 ports during the next horizontal scanning period. A total of 480 signals is read out, adding up the R, G and B channels. They are bit-serially converted to reduce their total number and then sent to the recording block. The system controller and circuitry necessary for generating the timing pulse and bias that drive the sensor are placed in the image sensing block.

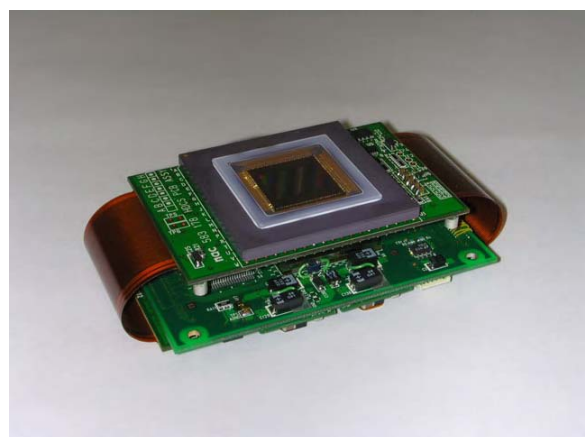


Photo 2: Image Sensing Device

Optical Block

Taking the number of pixels for HDTV (1920H x 1080V) from the sensor used, an image of 15.4mm diameter is acquired. As far as sensitivity is concerned, the use of a 1-inch pickup lens and color separation

